METHOD AND APPARATUS FOR INTERLEAVED GRAPHICS PROCESSING

ABSTRACT OF THE DISCLOSURE

The present invention provides for programmable interleaved graphics processing. The invention provides an execution pipeline and a number of registers. Each register holds instructions from a separate program. Instructions from the registers are interleaved in the execution pipeline such that the average latency is one instruction per cycle. This is accomplished even when there is conditional branching and execution latency. When one instruction has a dependency based on execution of a previous instruction, that second instruction is not provided to the execution pipeline until completion of the first instruction. However, in the meantime interleaved instructions from other programs are still being executed while the first instruction of the first program is executing. Thus the pipeline is always full and the processor is always working at peak capacity. The automatic interleaving of instructions permits simplified graphics software routines to be written. There is no need for the programmer or developer to anticipate or attempt to eliminate conditional branching or to worry about instruction latency. The design of the programmable interleaved graphics processing system provides a solution to those problems.